Claims

[c1] 1.A method of forming a semiconductor device with increased latch-up robustness, the method comprising:
providing a p-type semiconductor substrate;
locating within said substrate an I/O pad having no direct connection to n-diffusions;
forming within said substrate an n-well;
forming within said n-well a silicide blocked p-type field effect transistor having a snapback voltage that is less than the breakdown voltage of the gate oxide of said transistor.

[c2] 2.An ESD device comprising:
a silicide blocked p-type field effect transistor having a source, drain, gate, and gate oxide, said transistor further having a snapback voltage that is less than the breakdown voltage of said gate oxide and wherein said transistor is coupled to an I/O pad having no n-diffusions connected directly to it.

[c3] 3.The ESD device of claim 2 wherein said source is coupled to a voltage and said gate is coupled to said source and said drain is coupled said I/O pad.

[c4] 4.The ESD device of claim 2 further having a body terminal.

[c5] 5.The ESD device of claim 4 wherein said body terminal is coupled to said source.

[c6] 6.The ESD device of claim 2 wherein said snapback voltage is at most 5 volts.

[c7] 7.The ESD device of claim 2 wherein a p-type resistor is coupled to said transistor and coupled said I/O pad.

[c8] 8.The ESD device of claim 7 wherein said resistor is formed of p-type polysilicon.

[c9] 9.The ESD device of claim 7 wherein said resistor is a diffusion resistor.

[c10] 10.The ESD device of claim 7 wherein said p-type resistor is located between said transistor and said I/O pad so that a first voltage appearing at said I/O pad is of a different magnitude than a second voltage appearing at said transistor, said first and second voltages differing by a value proportional to the resistance of said p-type resistor.

[c11] 11.A latch-up robust integrated circuit comprising:
one or more I/O cells each having one or more I/O pads with no n-diffusions directly connected and wherein

each of said one or more I/O pads is coupled to an associated and distinct one or more silicide blocked p-type field effect transistors having a source, drain, gate, and gate oxide, said transistor further having a snapback voltage that is less than the breakdown voltage of said gate oxide.

[c12] 12.The latch-up robust integrated circuit of claim 11 wherein each of said one or more I/O pads is coupled said drain of said associated and distinct one or more transistors and said source of said transistors is coupled to a voltage and said gate is coupled to said source.

[c13] 13.The latch-up robust integrated circuit of claim 12 wherein each of said transistors has a body terminal.

[c14] 14.The latch-up robust integrated circuit of claim 13 wherein said body terminal of each of said transistors is coupled to said source.

[c15] 15.The latch-up robust integrated circuit of claim 11 wherein said snapback voltage of each of said transistors is at most 5 volts.

[c16] 16.The latch-up robust integrated circuit of claim 11 wherein one or more p-type resistors is coupled to one or more of each of said one or more I/O pads.

[c17] 17.The latch-up robust integrated circuit of claim 16 wherein each of said one or more p-type resistors is formed of p-type polysilicon.

[c18] 18.The latch-up robust integrated circuit of claim 16 wherein each of said one or more p-type resistors is a diffusion resistor.

[c19] 19.The latch-up robust integrated circuit of claim 16 wherein at least one of said one or more p-type resistors is located between the pad and associated transistor of each of said I/O pads so that a first voltage appearing at any of said I/O pads is of a different magnitude than a second voltage appearing at the associated transistor, said first and second voltages differing by a value proportional to the resistance of the p-type resistor.